

WHAT IS CLAIMED IS:

1. A semiconductor device comprising semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line, a stress cushioning layer installed on said semiconductor elements, a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an opening formed in said stress cushioning layer on said electrode pad, external electrodes arranged on said lead wire portion on said top of said stress cushioning layer, and a conductor protective layer installed on said stress cushioning layer excluding said external electrode arranged portion and on a conductor portion, wherein said stress cushioning layer, said lead wire portion, said conductor protective layer, (and said external electrodes have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said scribe line.)
2. A semiconductor device according to Claim 1, wherein said end face of said conductor protective

player is formed inside said end face of said stress cushioning layer.

3. A semiconductor device according to Claim 1,
5 wherein said end face of said conductor protective player is formed outside said end face of said stress cushioning layer.

4. A semiconductor device according to any of Claims 1
10 to 3, wherein an end area of said stress cushioning layer is formed so as to become taperingly thinner toward the said end face.

5. A semiconductor device comprising semiconductor
15 elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line, a semiconductor element protective layer installed on said semiconductor elements, a stress cushioning layer
20 installed on said semiconductor element protective layer, a first opening formed in said semiconductor element protective layer on said electrode pad, a second opening formed in said stress cushioning layer on said electrode pad, a lead wire portion extending
25 to a top of said stress cushioning layer through said

first opening and said second opening respectively
from said electrode pad, external electrodes arranged
on said lead wire portion on said top of said stress
cushioning layer, and a conductor protective layer
5 installed on said stress cushioning layer excluding
said external electrode arranged portion and on said
conductor portion, wherein said semiconductor element
protective layer, said stress cushioning layer, said
lead wire portion, said conductor protective layer,
10 and said external electrodes have means for forming
each end face on an end surface of said semiconductor
elements inside a cutting scribe line and exposing a
range from said end face on said end surface of said
semiconductor elements to an inside of said scribe
15 line.

6. A semiconductor device according to Claim 5,
wherein said end face of said conductor protective
12 player is formed inside said end face of said stress
20 cushioning layer.

7. A semiconductor device according to Claim 5,
wherein said end face of said conductor protective
25 player is formed outside said end face of said stress
cushioning layer.

8. A semiconductor device according to Claim 6 or 7,
wherein said end face of said semiconductor element
protective player is formed outside said end face of
said stress cushioning layer.

9. A semiconductor device according to Claim 6 or 7,
wherein said end face of said semiconductor element
protective player is formed inside said end face of
said stress cushioning layer.

10. A semiconductor device according to any of Claims
4 to 9, wherein an end area of said stress cushioning
layer is formed so as to become taperingly thinner
toward the said end face.

11. A semiconductor device manufacturing method
comprising a first step of forming a plurality of
semiconductor elements having an integrated circuit
and an electrode pad on a circuit forming surface of a
semiconductor wafer, a second step of forming a stress
cushioning layer on a plurality of semiconductor
elements, a third step of forming an opening in an
electrode pad of said stress cushioning layer and
forming a notch wider than a width of a scribe line in

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cont

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said stress cushioning layer on said cutting scribe line of said semiconductor wafer, a fourth step of forming a lead wire portion extending from said electrode pad to said stress cushioning layer via said opening, a fifth step of forming a conductor protective layer which covers said stress cushioning layer and said lead wire portion and has an external electrode connection window portion on said lead wire portion and a notch at a position corresponding to a notch of said stress cushioning layer, a sixth step of forming an external electrode in said external electrode connection window portion, and a seventh step of cutting said semiconductor wafer along said cutting scribe line and obtaining a plurality of semiconductor devices in minimum units.

12. A semiconductor device manufacturing method according to Claim 11, wherein an end face obtained by said notch of said conductor protective layer at said Step 5 is formed inside said semiconductor wafer cutting scribe line.

13. A semiconductor device manufacturing method according to Claim 12, wherein said end face obtained by said notch of said conductor protective layer at

said Step 5 is formed inside an end face formed by said notch of said stress cushioning layer.

14. A semiconductor device manufacturing method
5 according to Claim 12, wherein said end face obtained by said notch of said conductor protective layer at said Step 5 is formed outside an end face formed by said notch of said stress cushioning layer.

10 15. A semiconductor device manufacturing method comprising a first step of forming a plurality of semiconductor elements having an integrated circuit and an electrode pad on a circuit forming surface of a semiconductor wafer, a second step of forming a
15 semiconductor element protective layer on a plurality of semiconductor elements, a third step of forming a first opening in an electrode pad of said semiconductor element protective layer and forming a notch wider than a width of a scribe line in said
20 semiconductor element protective layer on said cutting scribe line of said semiconductor wafer, a fourth step of forming a stress cushioning layer on said semiconductor element protective layer, a fifth step of forming a second opening in said electrode pad of
25 said stress cushioning layer and forming a notch at a

position corresponding to a notch of said semiconductor element protective layer in said stress cushioning layer on said cutting scribe line of said semiconductor wafer, a sixth step of forming a lead wire portion extending from said electrode pad to said stress cushioning layer via said first opening and said second opening, a seventh step of forming a conductor protective layer which covers said stress cushioning layer and said lead wire portion and has an external electrode connection window portion on said lead wire portion and a notch at a position corresponding to said notch of said stress cushioning layer, an eighth step of forming an external electrode in said external electrode connection window portion, and a ninth step of cutting said semiconductor wafer along said cutting scribe line and obtaining a plurality of semiconductor devices in minimum units.

16. A semiconductor device manufacturing method according to Claim 15, wherein an end face obtained by said notch of said stress cushioning layer at said Step 4 is formed inside said semiconductor wafer cutting scribe line.

17. A semiconductor device manufacturing method

according to Claim 16, wherein said end face obtained by said notch of said stress cushioning layer at said Step 4 is formed inside an end face formed by said notch of said semiconductor element protective layer.

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18. A semiconductor device manufacturing method according to Claim 16, wherein said end face obtained by said notch of said stress cushioning layer at said Step 4 is formed outside an end face formed by said notch of said semiconductor element protective layer.

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19. A semiconductor device manufacturing method according to Claim 16, wherein said end face obtained by said notch of said stress cushioning layer at said Step 4 is formed so as to be installed on the same plane as that of an end face formed by said notch of said semiconductor element protective layer.

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20. A semiconductor device manufacturing method according to Claim 15, wherein an end face obtained by said notch of said conductor protective layer at said Step 7 is formed inside said semiconductor wafer cutting scribe line.

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21. A semiconductor device manufacturing method

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according to Claim 20, wherein said end face obtained
by said notch of said conductor protective layer at
said Step 7 is formed inside an end face formed by
said notch of said semiconductor element protective
5 layer.

22. A semiconductor device manufacturing method
according to Claim 20, wherein said end face obtained
by said notch of said conductor protective layer at
10 said Step 7 is formed outside an end face formed by
said notch of said semiconductor element protective
layer.

23. A semiconductor device manufacturing method
15 according to Claim 20, wherein said end face obtained
by said notch of said conductor protective layer at
said Step 7 is formed so as to be installed on the
same plane as that of an end face formed by said notch
of said semiconductor element protective layer.

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24. A semiconductor device manufacturing method
according to Claim 16 or 20, wherein said end face
obtained by said notch of said conductor protective
layer at said Step 7 is formed inside an end face
25 formed by said notch of said semiconductor element

protective layer and an end face formed by said notch of said stress cushioning layer.

25. A semiconductor device manufacturing method
5 according to Claim 16 or 20, wherein said end face obtained by said notch of said conductor protective layer at said Step 7 is formed outside an end face formed by said notch of said semiconductor element protective layer and an end face formed by said notch
10 of said stress cushioning layer.

26. A semiconductor device manufacturing method
according to Claim 16 or 20, wherein said end face obtained by said notch of said conductor protective
15 layer at said Step 7 is formed between an end face formed by said notch of said semiconductor element protective layer and an end face formed by said notch of said stress cushioning layer.

20 27. A semiconductor device manufacturing method according to Claim 16 or 20, wherein said end face obtained by said notch of said conductor protective layer at said Step 7 is formed to be installed on the same plane as that of an end face formed by said notch
25 of said semiconductor element protective layer and an

end face formed by said notch of said stress cushioning layer.

1. A method of forming a stress cushioning layer on a substrate, comprising the steps of: (a) providing a substrate; (b) providing a stress cushioning layer on the substrate; (c) forming a notch in the stress cushioning layer; and (d) forming an end face of the stress cushioning layer by the notch.